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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,501	01/20/2004	Daniel Eddleman	LT-170	4096

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EXAMINER	
AMAYA, CARLOS DAVID	
ART UNIT	**PAPER NUMBER**
2836	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/761,501	EDDLEMAN, DANIEL	
	Examiner	Art Unit	
	Carlos Amaya	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-11* is/are allowed.

6)☒ Claim(s) *12-14,16-18 and 20* is/are rejected.

7)☒ Claim(s) *15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to amendments filed on 11/14/2006.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 12-14, 16-18, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nercessian (US 3,623,140) in view of Arbetter (US 6,191,569).

With respect to claim 12 Nercessian discloses a method for controlling an output of a slave supply circuit (Slave supply 1) in a defined relationship to a time- varying master signal (Figure 2 shows a master and slave programmable power supplies, the master signal varies in time with respect to variable resistor 28, 14 and Programming voltage source 15), the slave supply circuit having a slave output terminal (Slave output terminal 4) and a feedback input terminal (Slave supply inverting input 2), the method comprising: accepting the master signal at a master supply circuit, the master signal varying at a master ramp rate (The master signal is varied by varying the resistance of resistor 14, 28 and Programming voltage source 15 Figure 2); generating current responsive to the master signal (Column 2 lines 66-72); forcing the output of the slave supply to vary responsive to the master signal and in accordance with the defined relationship (Column 2 lines 66-69); and presenting a high impedance to the feedback input terminal of the slave supply (the impedance of the feedback input terminal of the

slave supply is determined by the master supply 8, which depends on the varying master signal, thus to have high impedance the resistors 14, 28 and the programming voltage source 15 have to be taken into account).

Nercessian, however, does not disclose expressly injecting the generated current from the master supply circuit into the feedback input terminal of the slave supply circuit.

Arbetter discloses power supplies connected in parallel using a master/slave paralleling scheme, with feedback to maintain a regulation signal close to that of the master signal. Arbetter discloses that one of the power supply modules 20 can act as a master power supply that controls the other power supplies acting as slave supply, moreover there is a master signal in the Ishare bus injected to the slave power supply feedback circuit 28. Figure 2 shows a circuit 30 an embodiment of feedback circuit 28, with a feedback circuit 38 to generate a signal indicative of the difference between the master control signal and the local control signal col. 5 lines 1-5.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Nercessian with the teachings of Arbetter with master signal being injected on the feedback of a slave power supply.

The suggestion or motivation for doing so would have been to generate a slave signal that is indicative of a master control signal as disclosed by Arbetter.

With respect to claim 13 Nercessian in view of Arbetter disclose the method of claim 12, further comprising changing the ramp rate of the master signal with respect to time (The ramp rate signal and thus the output of the master supply 8 is change with

respect to resistors 14, 28 and voltage source 15, thus by changing one of the parameters the signal is change with respect to time).

With respect to claim 14 Nercessian in view of Arbetter disclose the method of claim 12, wherein forcing the output of the slave supply to vary comprises forcing the output of the slave supply to ramp at the same rate as the master ramp rate (By changing the master signal this signal in turns changes the output of the slave supply at the same rate, Column 2 lines 66-69).

With respect to claim 16 Nercessian in view of Arbetter disclose the method of claim 12, further comprising user-programming the defined relationship (Figure 2 shows a master and slave programmable power supplies, the user programs/changes the resistors 14, 28 and voltage source 15).

With respect to claim 17 Nercessian in view of Arbetter disclose the method of claim 16, wherein user- programming the defined relationship comprises selecting at least one resistance value (Either of resistor 14 or 28 can be selected /change by a user).

With respect to claim 18 Nercessian in view of Arbetter disclose the method claim 12, further comprising of generating the master signal. The master signal is generated with respect to resistors 14, 28 and programming voltage source 15.

With respect to claim 20 Nercessian discloses a method for controlling an output of a power supply in a defined manner, the method comprising: providing a power supply (Master power supply 8) with a feedback terminal (Feedback terminal consisting of variable resistor 28 connected to leads 29 and 30 and load terminal 21), an output

terminal (Load terminal 21) and a feedback network coupled between the feedback terminal and the output terminal (Feedback terminal and the output terminal are couple together as shown in Figure 2), the feedback network presenting a resistance (resistor 28) between the output terminal and the feedback terminal; and modifying the output of the power supply responsive to the dynamically changing resistance of the feedback network (Depending upon the resistance 28 the master supply is changed, Column 3 lines 4-8).

Nercessian, however, does not disclose expressly dynamically changing the resistance of the feedback network responsive to a digital input indicative of a master signal.

Arbetter discloses in figure 2 a circuit 30 an embodiment of feedback circuit 28, with a feedback circuit 38 to generate a signal indicative of the difference between the master control signal and the local control signal col. 5 lines 1-5.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Nercessian with the teachings of Arbetter with master signal being digital injected on the feedback of a slave power supply in the Ishare bus.

The suggestion or motivation for doing so would have been to generate a slave signal that is indicative of a master control signal, that is digital injected on the feedback of a slave supply as disclosed by Arbetter.

Allowable Subject Matter

1. Claims 1-11 are allowed over the prior art of record, because the prior art of record does not disclose or suggest "a charging circuit for supplying a drive signal to a ramp generator circuit configured to generate the master signal, the charging circuit having first and second current sources for selectably sourcing current to or sinking current from the ramp generator circuit; a tracking input terminal for receiving a tracking signal responsive to the master signal" and "a third current source coupled to the circuit output terminal that generates output current responsive to the op amp output signal, the output current having a magnitude that forces the output of the slave supply to behave in the defined relationship to the master signal when the circuit output terminal is coupled the feedback input terminal, and the coupling of the third current source to the circuit output terminal presenting a high impedance to the feedback input terminal". Along with the remaining features of the claim.

2. Claim 15 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

3. Claim 15 is allowable over the prior art of record, because the prior art of record does not disclose, "adding a time delay between onset of ramping the master signal and onset of ramping the output of the slave supply".

Conclusion

4. Applicant's arguments with respect to claims 12-18 and 20 have been considered but are moot in view of the new ground(s) of rejection.

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carlos Amaya whose telephone number is (571) 272-8941. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272-2800. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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